What is claimed is:

1. A method for controlling the top width of a trench, comprising the steps of:

providing a substrate, having a trench formed therein;

forming a conductive layer in a portion of the trench;

forming an interval layer in a portion of the trench, which in the interval layer in over the conductive layer;

forming a sacrificial layer on the sidewall of the trench over the interval layer;

removing the interval layer, exposing the underlying sidewall of the trench; and

oxidizing the sacrificial layer and the exposed sidewall of the trench.

2. The method according to claim 1, wherein the substrate is a single crystal silicon substrate.

3. The method according to claim 1, wherein the step of forming the conductive layer further comprises depositing the conductive layer over the substrate and in the trench and etching back the conductive layer, which in the top of the recessed conductive layer is below the surface of the substrate.

4. The method according to claim 1, wherein the conductive layer is formed of polysilicon.

5. The method according to claim 1, wherein the trench further comprises a capacitor.

6. The method according to claim 1, wherein the interval layer is formed of TEOS.

7. The method according to claim 1, wherein the steps of forming the interval layer further comprises depositing the

interval layer on the substrate and in the trench and etching back the interval layer, which in the top of the interval layer is below the surface of the substrate.

8. The method according to claim 1, wherein the method of forming the sacrificial layer further comprises conformally depositing the sacrificial layer on the interval layer and etching back the sacrificial layer to form the sacrificial layer on the sidewall of the trench over the interval layer.

9. The method according to claim 1, wherein the sacrificial layer is formed of polysilicon.

10. The method according to claim 1, wherein the depth of the trench is between 5000nm~9000nm.

11. A method for controlling the upper width of a trench, comprising:

providing a substrate, further comprising a trench;

forming a conductive layer in a portion of the trench;

forming a interval layer in a portion of the trench, where in the interval layer is over the conductive layer;

forming a shield layer on the sidewall of the trench over the interval layer;

removing the interval layer, exposing the sidewall of the trench over the conductive layer; and

oxidizing the exposed trench sidewall using the shield layer as a mask.

12. The method according to claim 11, wherein the substrate is a single crystal silicon substrate.

13. The method according to claim 11, wherein the step of forming the conductive layer further comprises depositing the conductive layer over the substrate and in the trench and

etching back the conductive layer, wherein the top of the recessed conductive layer is below the surface of the substrate.

14. The method according to claim 11, wherein the conductive layer is formed of polysilicon.

15. The method according to claim 11, wherein the trench further comprises a capacitor, and the conductive layer is used as the top electrode.

16. The method according to claim 11, wherein the interval layer is formed of TEOS.

17. The method according to claim 11, wherein the step of forming the interval layer further comprises depositing the interval layer on the substrate and in the trench and etching back the interval layer, in which the top of the interval layer is below the surface of the substrate.

18. The method according to claim 11, wherein the method of forming the shield layer further comprises conformally depositing the shield layer on the interval layer and etching back the shield layer to form the shield layer on the sidewall of the trench over the interval layer.

19. The method according to claim 11, wherein the shield layer is formed of silicon nitride.

20. The method according to claim 11, wherein the depth of the trench is between 5000nm~9000nm.